the poly-Si after the top oxide is deposited and planarized down to expose only these top surfaces.

Figure 2(h) illustrates that finally the HDP oxide 90 is deposited over the poly pillars, and the top oxide HDP is removed (e.g. polished) down to the tops of the poly pillars, as discussed in co-pending United States Patent Application Serial No. 09/675,435 .

Amend the paragraph on page 11, lines 9-11, as follows.

Nitride liner is easily removed from the top surface when combined with method disclosed in co-pending United States Patent Application Serial No. 09/675,435 to avoid complications with CB etch.

IN THE CLAIMS:

1. (Amended) A DRAM cell array which comprises:

a plurality of memory cells which are arranged in rows and columns, each memory cell including a deep trench region having a vertical MOSFET and an underlying capacitor formed therein that are in electrical contact to each other through at least one buried-strap outdiffusion region which is present within a portion of a wall of each deep trench; and,

each memory cell having a deep trench conductor forming an electrode of said underlying capacitor and a collar oxide region formed in a portion of the deep trench;

the collar oxide region formed on a remaining wall portion of each deep trench not containing said buried-strap outdiffusion region for electrically isolating a body [contact] region from said underlying capacitor; and

a trench top oxide (TTO) layer formed on a horizontal surface of the DRAM cell array for isolating the deep trench conductor forming an electrode of said underlying capacitor and said buried-strap outdiffusion region from a gate conductor region;

an underlying nitride layer formed between a top of said deep trench conductor and said buried-strap outdiffusion region and underlying said TTO layer to eliminate a possibility of TTO layer dielectric breakdown between said gate conductor region and said electrode of said underlying capacitor.

2. (Amended) The DRAM cell array of Claim 1, wherein said TTO layer is formed on sidewalls of the DRAM cell array and said horizontal surface, wherein said underlying nitride layer is formed to line said sidewalls to protect said collar oxide region and prevent said buried-strap outdiffusion region from being etched during a TTO oxide sidewall etch .

3. (Amended) The DRAM cell array of Claim 1, further including a sacrificial oxide layer formed underneath said nitride layer to further eliminate a possibility of TTO layer dielectric breakdown between the gate conductor region and said deep trench conductor.

4. (Amended) The DRAM cell array of Claim 1, wherein said nitride layer is deposited to a thickness ranging from 1.0 nm – 10.0 nm.

5. (Amended) The DRAM cell array of Claim 1, wherein each said vertical MOSFET includes gate dielectrics formed on inner surfaces of said sidewalls of each said deep trench.